



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Matthew Von Thun
Brian Burdick
Edson Porter

Serial No. : 10/068,768

Group Art Unit : 2816

Filed : February 06, 2002

Examiner : Le, Dinh

For : Five volt tolerant and fail safe input
scheme using source follower
configuration

Atty Docket : 1496.00201 / 02-0003

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

June 21, 2004 
Date Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

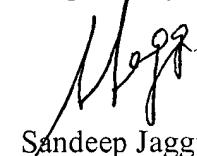
Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Date: 6/18/04

Respectfully submitted,


Sandeep Jaggi

Reg. No. 43,331